In the Claims:

1-7. (canceled)

8. (previously presented) A modulator circuit comprising:

a memory for storing interleaved data, the memory having a write address port and a read address input port;

an inverse interleaving address generator coupled to the write address port; and

a range selector circuit having an input port for receiving a pseudonoise (PN) index or a reverse link frame timing signal and an output port for providing a read address to the memory.

9-25. (canceled)

26. (new) The modulator circuit of claim 8 in which the reverse link frame timing signal includes a counter signal, and the range selector circuit includes a range select input that selects a desired range of the counter signal.

27. (new) The modulator circuit of claim 8 in which the reverse link frame timing signal includes a counter signal that changes state at a chip rate.

28 (new) The modulator circuit of claim 8 in which the reverse link frame timing signal includes a counter signal, the range selector circuit includes a range select input that selects a desired range of the counter

signal, and the output port of the range selector circuit provides a read address [n:0] = counter signal [(n+2):2].